IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Canceled).

Claim 2 (Currently Amended): An audio processor according to claim [[1]] 35, wherein the coprocessor is configured to subserve the control processor to subject sequentially the audio data to decoding, noise-less decoding, noise reduction, filter bank, and block switching in accordance with the programs and data fetched from the external memory in units of one procedure.

Claim 3 (Previously Presented): An audio processor according to claim 2, wherein the coprocessor is configured to subserve the control processor to execute the program fetched in the internal memory from the external memory in accordance with progress of the procedures of the audio process.

Claims 4-7 (Cancelled).

Claim 8 (Currently Amended): An audio processor according to claim [[1]] 35, wherein the control processor sequentially transfers a plurality of program modules corresponding to ~~procedures~~ processes of the audio process to the coprocessor from the external memory according to the progress of the ~~procedures~~ processes.

Claim 9 (Currently Amended): An audio processor according to claim [[1]] 35, wherein the coprocessor subserves the control processor to execute decoding of bit stream data, noiseless decoding, inverse quantization, scale factor, TNS processing, filter bank processing, and the block switching, in this order, to reconstruct audio data.

Claim 10 (Currently Amended): An audio processor according to claim 9, wherein the control processor includes a function of predicting which ~~procedure~~ process is performed after the ~~procedures~~ process which is currently performed.

Claim 11-13 (Cancelled).

Claim 14 (Currently Amended): An audio processor according to claim [[1]] 35 wherein the control processor is further configured to release a storage region of the internal memory occupied by the data stored in the internal memory or a program if the data stored in the internal memory or the program becomes unused by the coprocessor.

Claims 15-23 (Cancelled).

Claim 24 (Currently Amended): The audio processor according to claim [[1]] 35, ~~wherein the internal memory includes an instruction memory and a data memory, and~~ which further includes at least two parallel busses lead from the instruction memory and the data memory to the coprocessor.

Claims 25-29 (Cancelled).

Claim 30 (Currently Amended): The audio processor according to claim [[1]] 35, further comprising:

an audio input/output interface; and

an internal bus;

wherein the internal bus links the control processor, the coprocessor and the audio input/output interface together.

Claims 31-33 (Cancelled).

Claim 34 (Currently Amended): The audio processor according to Claim [[1]] 35, wherein the processes include five different processing stages performed sequentially, the five different processing stages using different memory spaces of the data memory in the internal memory.

Claim 35 (New): An audio processor which processes audio data via an external memory configured to store audio data and a plurality of programs corresponding to a plurality of processes which are to be sequentially executed in a given order for processing the audio data, the audio processor comprising:

an instruction memory configured to store a program corresponding to each of the processes;

a data memory configured to store audio data;

a DMA controller configured to DMA-transfer a program and audio data from the external memory to the instruction memory and the data memory;

a control processor configured to execute the program transferred to the instruction memory along with a progress of each of the processes, and request, while continuing a process which is currently executed, audio data and a program that are required for a next process to the DMA controller; and

a coprocessor configured to increase performance of reconstruction of the audio data obtained via the control processor according to the program given by the control processor, and execute multiplication/accumulation addition according to VLIW (Very Long Instruction Word);

wherein the control processor controls in such a manner that when a k-th (k is integer) process is started, the content of the data memory unnecessary for the k-th process out of a k-1-th process results is saved in the external memory, the program required for a k+1-th process and data are transferred to the instruction memory and the data memory from the external memory.